MSME-TOOL ROOM, HYDERABAD
CENTRAL INSTITUTE OF TOOL DESIGN

VES COURSES
2015-2016

[Images of electronic components and diagrams related to technology]
PG Diploma in VLSI & Embedded Systems (PGDVES) + M.Tech Project Work

- **Programming**: Verilog, VHDL Languages.
- **Digital Design**: Combinational & Sequential Designs, Low power VLSI Design, High speed VLSI Design.
- **Front End Design**: RTL Coding, Constraints Design, Library exploring, Synthesis.
- **Physical Design**: Design Import, Sanity checks, Flour planning, Power planning, Placement, CTS, Routing, Sign off Verification.
- **Analog Circuit Design**: Basic Designs of CMOS circuits, Layout Design, DRC, LVS.
- **SOC Verification**: Functional Verification.

**PROJECT WORK**

Course Fee: Rs. 55,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 84,000/- + 500/- Reg. Fee for Govt. Org. & Major Industries.
Fee can be paid in 2 installments.


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**Embedded Systems**

- **Introduction**: Overview of Embedded Systems, Firmware concept, Embedded Software, Embedded C Programming, Compiler
- **Microcontrollers**: 8051, AVR, PIC, ARM7.
- **Interfacing**: 5x7 Matrix display, Keypad, LCD, ADC, DAC, Sensors, RFID, GSM and GPS
- **RTOS**: Embedded Linux, Vx Works.

**PROJECT WORK**

Course Fee: Rs. 55,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 84,000/- + 500/- Reg. Fee for Govt. Org. & Major Industries.
Fee can be paid in 2 installments.

CMOS Analog Circuit Design (CACD)

- Basic Design of CMOS Circuits: nMOS logic, pMOS logic, CMOS logic.
- Schematic Design: Virtuoso schematic editor.
- Power Analysis in CMOS: AC and DC power analysis for designs.

Course Fee: Rs. 24,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 53,000/- + 500/- Reg. Fee for Govt. Org. & Major industries.


Advanced Digital System Design

- SOC Verification: Functional Verification.

Course Fee: Rs. 19,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 28,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

Digital Design in VLSI (DVD)

- **Digital Electronics** : Combinational and Sequential Designs.
- **Programming** : Verilog and VHDL Languages
- **Hardware** : CPLD & FPGA

**Course Fee:** Rs. 19,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 28,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

Eligibility: Diploma/BSc ECE/EIE equivalent.

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Embedded Systems

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**Course Fee:** Rs. 19,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 28,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

SOC Verification

**UVM**: UVM, Transaction level Modeling, Developing Reusable Verification Components, Using Verification Components.

**UVM+**: The Built-In Factory and Overrides, callbacks, the Sequence Laboratory, Advance Sequence Control, UBUS Verification Component Architecture.

Course Fee: Rs. 13,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 22,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

BE/B.Tech/MSc ECE/EIE equivalent.

Verilog and VHDL

**Verilog & VHDL Languages**: Behavioral modelling, Gate level modelling, Structural modelling.

Course Fee: Rs. 13,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 22,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

BE/B.Tech/MSc ECE/EIE equivalent.

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VHDL

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity LATCH_6 is
port (EN1, EN2, E0, E1, A1, A2, A3, A4, A5, A6 : in std_logic;
      I1 : in std_logic;
      Y : out std_logic);
end entity LATCH_6;

architecture RTL of LATCH_6 is
begin
process (EN1, EN2, E0, E1, A1, A2, A3)
begin
if (EN1 = '1') then
  case (E0, E1) is
    when '00' | '11' => Y <= A1;
    when '01' => Y <= A2;
    when '10' => Y <= A3;
    when others => Y <= A4;
  end case;
end if;
end process;
end architecture RTL;
```

Verilog

```verilog
module LATCH_6 (I1, E0, E1, A1, A2, A3, A4, A5, A6);
  input EN1, EN2, E0, E1, A1, A2, A3;
  output Y;
  reg Y;
  always @(E0 or E1 or EN1 or A2 or A3)
    begin
      if (EN1 == '1')
        Y <= A1;
      else
        if (E0 == '1')
          Y <= A2;
        else
          Y <= A3;
        end if;
    end if;
endmodule
```
1 Month - 3hrs a day

**Verilog**

- **Verilog Language**: Behavioral modelling, Gate level modelling, Structural modelling.

  - **Course Fee**: Rs. 6,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 7,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.
  - **Eligibility**: ME/M.Tech Pursuing in ECE/EIE/VLSI/ES/DECS/DSP Equivalent. BE/B.Tech/MSc ECE/EIE equivalent.

**VHDL**

- **VHDL Language**: Behavioral modelling, Gate level modelling, Structural modelling.

  - **Course Fee**: Rs. 6,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 7,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.
  - **Eligibility**: ME/M.Tech Pursuing in ECE/EIE/VLSI/ES/DECS/DSP Equivalent. BE/B.Tech/MSc ECE/EIE equivalent.

**8051 MICROCONTROLLER**

- **Embedded C**
- **8051 Architecture**
- **Input/output Ports and Circuits**
- **External Memory**
- **Counters**
- **Timers**
- **Serial Communication**
- **Interrupts**

  - **Course Fee**: Rs. 6,000/- + 500/- Reg. Fee for SME & Individuals, Rs. 7,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.
  - **Eligibility**: ME/M.Tech Pursuing in ECE/EIE/VLSI/ES/DECS/DSP Equivalent. BE/B.Tech/B.Sc/M.Sc ECE/EIE Pursuing or equivalent.
### PIC Micro Controller

**Introduction**
- Overview of Embedded Systems, Firmware concept,
- Embedded Software, Embedded C Programming, Compiler

**Microcontrollers**
- PIC

**Interfacing**
- 5x7 Matrix display,
- Keypad, LCD,
- ADC, DAC,
- Sensors,
- RFID, GSM and GPS

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**Course Fee:** Rs. 6,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 7,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

**Eligibility:** ME/M.Tech Pursuing in ECE/EIE/VLSI/ES/DECS/DSP Equivalent.
BE/B.Tech/MSc ECE/EIE equivalent.

### ARM 7

**Introduction**
- Overview of Embedded Systems, Firmware concept,
- Embedded Software, Embedded C Programming, Compiler
- Register Programming

**Microcontrollers**
- ARM 7 (LPC 2148)

**Interfacing**
- 5x7 Matrix display,
- Keypad, LCD,
- ADC, DAC,
- Sensors.

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**Course Fee:** Rs. 6,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 7,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

**Eligibility:** ME/M.Tech Pursuing in ECE/EIE/VLSI/ES/DECS/DSP Equivalent.
BE/B.Tech/MSc ECE/EIE equivalent.
RTOS

- Introduction to Operating Systems
- Semaphores
- Kernels
- Linux Programming Using VxWorks

Course Fee: Rs. 6,000/- + 500/- Reg. Fee for SME & Individuals,
Rs. 7,500/- + 500/- Reg. Fee for Govt. Org. & Major industries.

BE/B.Tech/MSc ECE/EIE equivalent.

Note:

- All the above courses will be commenced on 1st & 3rd Wednesday of every month.
- For SC/ST Candidates fee waiver will be provided as per Govt. of Indian Norms.

Project Works

For Diploma Projects:
Fee: Rs.13,500/- + Rs.500/- Registration Fee per participant
(Verilog, VHDL, FPGA and CPLD Programming and Practical Training in the tool Rooms)
Duration: Six Months
(4 Months Theory and 2 Months Lab)

For B.E/B.Tech Projects:
Fee: Rs.5500/- + Rs. 500/- Registration Fee per participant
for any Two software with project.
Fee: Rs. 7500/- + Rs. 500/- Registration Fee per participant
for any Two software with project.
B.E/B-Tech Project Works Commence in December & January.

For PhD/Research Scholar’s Projects:
Fee: Rs.16,000/- + Rs.500/- Registration Fee per participant for utilization of our facilities (any two softwares and hardware) for about 300 hrs without guidance from the faculty. If any assistance is required by the participant then he/she has to register for the respective courses by paying the fee required.